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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/780,554	GATES ET AL.
	Examiner	Art Unit
	Alexander O. Williams	2826

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *12-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-11* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/780554 Attorney's Docket #: 20140-00318-US
Filing Date: 2/19/2004;

Applicant: Gates et al.

Examiner: Alexander Williams

Applicant's election of Species II, figure 2, filed 11/21/05 to the election of Group I (claims 1 to 11), filed 9/9/05, has been acknowledged.

This application contains claims 12 to 33 drawn to an invention non-elected without traverse.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 5, 9, 10 and 11 are rejected under 35 U.S.C. § 102(e) as being anticipated by Grunow et al. (U.S. Application Publication # 2005/0082089 A1).

1. Grunow et al. (figures 1A to 2^E) specificically figures 1D and 2E show a back end of the line (BEOL) interconnect structure **50,50a** comprising:

(a) an ultralow k (ULK) dielectric **16**, having a dielectric constant of up to about 3, and conductive metal **200,200a,402** features provided on a substrate **14**;

(b) a liner barrier layer **400** between said ULK dielectric and said conductive metal features; and

(c) a thin dielectric layer (TDL) **320**, having a thickness of up to about 5 nanometers, between the liner barrier layer and the ULK dielectric, wherein the TDL comprises a dense dielectric film having hermetic barrier capability, said film comprising a different material than the material of the ULK dielectric.

2. The interconnect structure of claim 1, Grunow et al. show wherein the TDL has a thickness ranging from about 0.5 nanometers to about 5 nanometers.

Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

3. The interconnect structure of claim 2, Grunow et al. show wherein the TDL exhibits conformal deposition and is essentially defect free.

4. The interconnect structure of claim 1, Grunow et al. show wherein the TDL has a thickness ranging from about 1 nanometer to about 3 nanometers and a conformality that is at least about 0.5.

Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

5. The interconnect structure of claim 4, Grunow et al. show wherein the TDL material is selected from the group consisting of silicon nitride (SiN), SiC, SiCH, SiNH, SiCNH, SiCOH, AlN, BN, SiCBN, CN, and alloys, mixtures, and multilayers of the same.

9. The interconnect structure of claim 5, Grunow et al. show wherein the liner barrier layer is selected from the group consisting of Ta, TaN, Ti, TiN, W, WN, and alloys, mixtures, and multilayers of the same; the ULK dielectric is selected from the group consisting of SiCOH and porous SiCOH materials with a dielectric constant ranging from about 1.5 to about 3.0; and the conductive metal features are selected from the group consisting of Cu, Al, Ag, Au, W, and alloys, mixtures, and multilayers of the same.

10. The interconnect structure of claim 9, Grunow et al. show wherein the liner barrier layer is selected from the group consisting of Ta, TaN, and alloys, mixtures, and multilayers of the same; and the conductive metal features comprise Cu.

11. The interconnect structure of claim 2, Grunow et al. show wherein the ULK dielectric has a dielectric constant ranging from about 1.5 to about 3.0; and the TDL has a dielectric constant ranging from about 2.8 to about 7.

[0039] FIG. 2C illustrates the undesirable results of going straight to Cu-seed and/or electrochemical deposition of the copper 402 to fill the vias 180, 180a and the trenches 200, 200a immediately following the etching process previously discussed. It can be seen from FIG. 2C that any misalignment 240, 240a of the vias 180, 180a with the first layer copper lines 100, 100a will provide an opportunity for copper diffusion from the vias 180, 180a into the dielectric layer 140. Without additional processing, the design rules for the circuit would have to be relaxed to overcome variations in the alignment tolerances of the photolithographic processing equipment. This would lead to increased manufacturing costs of the circuit.

[0040] Therefore, as illustrated in FIG. 2D, a second barrier deposition is performed that forms a barrier layer 400 over the walls of the vias 180, 180a including the bottom surface 400. This barrier is designed to have the characteristics necessary to protect against copper diffusion into dielectric 140 through misalignment 240, while exhibiting relatively low resistivity and increasing/providing sufficient wettability to copper. In one embodiment, the layer can be formed of tantalum using a flash deposition process in the same chamber as used to perform the selective etch to remove the diffusion barrier layer 320 (and the residues 210) from the bottom of the vias 180, 180a as illustrated in FIG. 2B. The conditions for the deposition can be the same as those used for deposition of the diffusion barrier layer 320 if a PVD Ta layer is used for the flash barrier 400. The flash layer 400 can range in thickness from 10-300 Angstroms with a typical range of 20-150 Angstroms. Other materials that may be used as the flash barrier layer 400 are TaN/Ta, Ru, or any other material that provides sufficient and/or increased wettability of copper, exhibits relatively low resistivity and provides a diffusion barrier against copper.

[0041] Finally, FIG. 2E illustrates the state o This disclosure describes methods and apparatus that address one or more of the issues noted above. In at least some embodiments, a via is formed between first and second layer copper lines by depositing a first barrier layer over the inner wall and bottom surfaces of the via, then selectively removing the first barrier layer from the bottom surface of the via, and then depositing a second layer made of material that also forms a barrier to copper

migration ensures sufficient wettability of copper and, is relatively less resistive than the first barrier layer. In at least some embodiments, the selective removal of the barrier layer from the bottom of the via may be performed in the same processing chamber as the deposition of the second layer.f the stacked structure 50, 50a after a Cu or Cu-alloy seed deposition and/or Cu ECD fill process that leads to the vias 180, 180a and trenches 200, 200a being filled with copper or copper alloy 402. As can be see, the flash barrier layer 400 on the bottoms of the vias 180, 180a provides a copper diffusion barrier to prevent migration through the misaligned areas 240, 240a. The flash barrier layer 400 further provides adequate if not improved wettability of the copper 402 to the barrier 400 of the vias 180, 180a and the trenches 200, 200a.

[0042] In summary, embodiments of the invention eliminate the need for the known PSE step in building stacked interconnect structures, which leads to the undesirable effects of flaring of the dielectric walls and re-sputtering of copper onto the walls of the structure prior to deposition of a diffusion barrier. Moreover, more flexibility is provided regarding the choices for materials and processes for forming the initial barrier layer. Thin conformal barrier layers with good diffusion barrier characteristics can be used despite their high resistivity because they are selectively etched from the bottom surfaces of the vias making contact with a first layer metal interconnect. Finally, any exposure to the dielectric layers through the selectively etched surface of the vias due to misalignment are sealed by way of a flash barrier deposition that not only acts as a diffusion barrier to migration of copper through the misaligned vias, but also provides sufficient and can improve wettability of the copper for adherence purposes and relatively low resistivity characteristics that facilitate good low-resistance contact between the first and second layer copper lines.

Claims 1 to 5 and 9 to 11 are rejected under 35 U.S.C. § 102(e) as being anticipated by Beyer et al. (U.S. Patent Application Publication # 2005/0074961 A1).

1. Beyer et al. (figures 1 to 13C) specifically figures 4a and 7a-7D show a back end of the line (BEOL) interconnect structure comprising:
(a) an ultralow k (ULK) dielectric **1**, having a dielectric constant of up to about 3, and conductive metal features provided on a substrate (SiO2);

(b) a liner barrier layer **5** between said ULK dielectric and said conductive metal features; and
(c) a thin dielectric layer (TDL) **4**, having a thickness of up to about 5 nanometers, between the liner barrier layer and the ULK dielectric, wherein the TDL comprises a dense dielectric film having hermetic barrier capability, said film comprising a different material than the material of the ULK dielectric.

2. The interconnect structure of claim 1, Beyer et al. show wherein the TDL has a thickness ranging from about 0.5 nanometers to about 5 nanometers.

Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

3. The interconnect structure of claim 2, Beyer et al. show wherein the TDL exhibits conformal deposition and is essentially defect free.

4. The interconnect structure of claim 1, Beyer et al. show wherein the TDL has a thickness ranging from about 1 nanometer to about 3 nanometers and a conformality that is at least about 0.5.

Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

5. The interconnect structure of claim 4, Beyer et al. show wherein the TDL material is selected from the group consisting of silicon nitride (SiN), SiC, SiCH, SiNH, SiCNH, SiCOH, AlN, BN, SiCBN, CN, and alloys, mixtures, and multilayers of the same.

9. The interconnect structure of claim 5, Beyer et al. show wherein the liner barrier layer is selected from the group consisting of Ta, TaN, Ti, TiN, W, WN, and alloys, mixtures, and multilayers of the same; the ULK dielectric is selected from the group

consisting of SiCOH and porous SiCOH materials with a dielectric constant ranging from about 1.5 to about 3.0; and the conductive metal features are selected from the group consisting of Cu, Al, Ag, Au, W, and alloys, mixtures, and multilayers of the same.

10. The interconnect structure of claim 9, Beyer et al. show wherein the liner barrier layer is selected from the group consisting of Ta, TaN, and alloys, mixtures, and multilayers of the same; and the conductive metal features comprise Cu.

11. The interconnect structure of claim 2, Beyer et al. show wherein the ULK dielectric has a dielectric constant ranging from about 1.5 to about 3.0; and the TDL has a dielectric constant ranging from about 2.8 to about 7.

[0041] Referring now to FIGS. 4A and 4B, the process of lining the sidewalls of the hole and the field a barrier layer 5 is illustrated. The barrier layer 5 may be deposited using Physical Vapor Deposition (PVD), Chemical Vapor Deposition (CVD), Metal Organic Chemical Vapor Deposition (MOCVD), Atomic Layer Deposition (ALD), or any other appropriate technique. Examples of materials that may be used for the barrier layer 5 are TaN, Ta, TiN, Ti, WN and WCN. The barrier layer 5 can act as diffusion barrier for HF during the formation of the airgaps.

[0042] The hole 3 is then filled with a conductive material 6, for example Cu, Au or Ag. Of course, conductive materials may be used, such as other metals, carbon nanotubes, carbon annotates and conductive polymers. The overburden of the conductive material, for example the overburden of Cu, and the overburden of any barrier layer on the field of the dielectric material 1 are removed by a subtractive technique. As is illustrated by FIGS. 5A and 5B, such subtractive technique are employed to only leaves the barrier layer 5 and the conductive material 6 that is within the hole in place. Any number of subtractive technique may be used, such as Chemical Mechanical Polishing (CMP), Electro Polishing, etch or any combination of these or other appropriate techniques. Additionally, the subtractive techniques may also remove the dielectric material 2, as shown in FIGS. 5A and 5B.

[0043] The conductive material 6 formed in the holes in the stack of layers may be horizontal lines (also referred to as "trenches") or vertical structures (also referred to as "vias"). The vias and trenches are part of a (single or dual) damascene structure that is formed during "end of line" processing a

semiconductor device. The airgaps that are created in a damascene structure may be formed near the vias and/or the trenches of the structure. However, leaving the dielectric material 1 intact near the via structures may provide more mechanical support and stability for the damascene structure.

[0044] The converted dielectric material 4 is then removed using an etch medium that is highly selective of the converted dielectric material 4 over the unconverted dielectric material 1. (e.g., etches the converted dielectric material 4 more rapidly). This etch selectivity is illustrated by FIGS. 6A and 6B. In this example, the removal of the converted dielectric material 4 is accomplished using an HF treatment. The HF treatment may be applied in any number of ways. For example, the converted dielectric material 4 may be exposed to vapor HF (VHF) or by dipping the layer stack (e.g., in wafer or die form) in a liquid HF solution. For example, an aqueous HF solution that contains less than 5% HF, less than 2% HF or around 1% HF may be used. Such solutions may have other HF concentrations and be prepared with/without additives, such as methanol. As another alternative, the layer stack may be subjected to a Super Critical CO.sub.2 (SCCO.sub.2) environment with the addition of HF.

[0045] Using such techniques, substantially complete removal of the converted dielectric material 4 will take place in smaller interconnect geometries (smaller interline spacing), such that the airgaps span substantially the complete width between 2 neighboring lines, as is shown in FIG. 6B. For example, substantially complete removal of the converted dielectric material 4 is possible in the case where two adjacent conductive (e.g., Cu) lines are spaced on the order of 50 nm from each other.

[0046] For this particular technique, the duration of the process of chemically and/or mechanically changing the properties of the first dielectric layer locally has a greater effect on the formation of airgaps than the duration of the applying the first etching substance To dissolve the first dielectric material around the conductive material 6. It will be appreciated that the process of chemically and/or mechanically changing the properties of the first dielectric layer locally will determine which area will be etched by the first etching substance, when applied.

[0047] The distance at which neighboring conductive lines may be place is determined, in part, by the limitations of techniques for forming neighboring holes in the stack of layers. Currently, metal lines are spaced at about 100 nm. The methods, devices and techniques described herein are relatively scaling invariant and are currently limited to any particular distance between conductor lines, as chemically and/or mechanically changing the properties of the liner layers locally may be readily accomplished on a nanometer scale and smaller.

[0048] If the distance between neighboring conductor lines is approximately 100 nm or less, it is possible to remove all the intermediate dielectric material and leave only an airgap in between. Such an approach is illustrated by FIGS. 3B, 4B, 5B and 6B. For distances larger then 100 nm, some dielectric material is left between the lines in order to provide mechanical support for the deposition of further layers on the top of the airgap structure described herein.

[0049] In certain embodiments, the methods described above may be repeated; such as forming new layers on top of an airgap structure. In a Dual Damascene (DD) interconnect structure, as illustrated in FIGS. 13A-13C, airgaps (7) are formed in the dielectric material near the vias (as shown in FIG. 13 (c)), near the trenches (as shown in FIG. 13(b)) or both (as shown in FIG. 13(a)). Most preferred is the formation of airgaps near the trenches and leave original dielectric material (1) near the via structure. Leaving the original dielectric material (1) near the via structures will give more mechanical support to the Dual Damascene structure.

EMPIRICAL EXAMPLES

Example 1

[0050] Referring now to FIGS. 10A-10C, a structure is depicted that was created by depositing Ultra Low-K (ULK) dielectric material for the dielectric material 1 and SiO.sub.2 for the dielectric material 2 using standard processing. Resist patterns were created using standard resist and standard 193 nm optical lithography. In order to create a hole, the resist pattern is transferred into the dielectric stack using a standard plasma etch system. The plasma contained argon, oxygen, and fluorocarbon molecules. The resist was ashed by a

plasma in a standard ash system using oxygen and fluorocarbon molecules. A TaN/Ta barrier layer 5 and conductive material 6 were deposited in the hole and on the field and subsequently removed from the field using a subtractive technique, as were previously discussed. The converted dielectric material 4 was then removed using diluted HF, which also resulted in the creation of airgaps 7 adjacent to the wires.

Example 2

[0051] An overall process for selectively integrating airgaps is shown in FIGS. 7A-7D. In FIG. 7A, a stack including a 50/200/50/275/13 nm Si.sub.3N.sub.4/SiO.sub.2/SiC/SiOC:H/SiO.sub.2 was formed on a 100 Si wafer using plasma enhanced chemical vapor deposition (PE-CVD). Patterning was done using 193 nm wavelength optical lithography. Dry etch and resist ash were carried out in a Lam Exelan2300.TM. chamber using a CF.sub.4/CH.sub.2F.sub.2/Ar/O.sub.2 plasma at low pressure and an O.sub.2/CF.sub.4 plasma at high pressure, respectively. Both dry etch and resist ash processes were carefully controlled in order to induce a defective SiO.sub.x film at the sidewalls of the SiOC:H trenches, as illustrated FIG. 7A.

[0052] Then a 15/10 nm Ta/Ta(N) diffusion layer and a 100 nm Cu seed layer were formed using ionized physical vapor deposition (i-PVD). Trenches were filled using copper electroplating and the excessive metal was removed using chemical mechanical polishing (CMP) to produce the stack shown in FIG. 7B. HF was then used to selectively dissolve the SiO.sub.x vs. the SiOC:H, which resulted in airgap formation at sidewalls, as is depicted in FIG. 7C. The HF dip time was controlled such that the SiO.sub.x layer was removed with relatively little degradation to the SiCO:H layer, the Ta/Ta(N) diffusion barrier and the Cu conductor. Subsequently a 50/330/500 nm SiC/SiO.sub.2/Si.sub.3N.sub.4 passivation layer was deposited on top of the layer stack, as illustrated in FIG. 7d.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a liner barrier layer and a thin dielectric layer deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1 to 5 and 8 to 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalton et al. (U.S. Patent Application Publication # 2005/0064701 A1).

1. Dalton et al. (figures 1 and 2) specifically figure 1 show a back end of the line (BEOL) interconnect structure comprising:

(a) an ultralow k (ULK) dielectric **3**, having a dielectric constant of up to about 3, and conductive metal features **5** provided on a substrate **10**;

(b) a liner barrier layer **(first layer of multiples layer of 6)** between said ULK dielectric and said conductive metal features; (Note: **The liner can be a single layer or it can include multiple layers)** and

(c) a thin dielectric layer (TDL) **(second layer of multiple layers of 6)**, having a thickness of up to about 5 nanometers, between the liner barrier layer and the ULK dielectric, wherein the TDL comprises a dense dielectric film having hermetic barrier

capability, said film comprising a different material than the material of the ULK dielectric.

2. The interconnect structure of claim 1, Dalton et al. show wherein the TDL has a thickness ranging from about 0.5 nanometers to about 5 nanometers.

Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

3. The interconnect structure of claim 2, Dalton et al. show wherein the TDL exhibits conformal deposition and is essentially defect free.

4. The interconnect structure of claim 1, Dalton et al. show wherein the TDL has a thickness ranging from about 1 nanometer to about 3 nanometers and a conformality that is at least about 0.5.

Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Initially, and with respect to claim 8, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103 in claim 8, see MPEP § 2113.
8. The interconnect structure of claim 1, Dalton et al. show wherein the TDL is deposited by a method selected from the group consisting of: high density plasma (HDP), downstream HDP, electron cyclotron resonance (ECR), plasma enhanced chemical vapor deposition (PE CVD), assisted PE CVD, and plasma enhanced atomic layer deposition (PE ALD).
9. The interconnect structure of claim 5, Dalton et al. show wherein the liner barrier layer is selected from the group consisting of Ta, TaN, Ti, TiN, W, WN, and alloys, mixtures, and multilayers of the same; the ULK dielectric is selected from the group consisting of SiCOH and porous SiCOH materials with a dielectric constant ranging from about 1.5 to about 3.0; and the conductive metal features are selected from the group consisting of Cu, Al, Ag, Au, W, and alloys, mixtures, and multilayers of the same.
10. The interconnect structure of claim 9, wherein the liner barrier layer is selected from the group consisting of Ta, TaN, and alloys, mixtures, and multilayers of the same; and the conductive metal features comprise Cu.
11. The interconnect structure of claim 2, wherein the ULK dielectric has a dielectric constant ranging from about 1.5 to about 3.0; and the TDL has a dielectric constant ranging from about 2.8 to about 7.

[0017] Accordingly, the present invention provides a general method of making a BEOL interconnect structure including a porous or dense low k dielectric having low via contact resistance. The method includes the steps of:

[0018] a) forming a porous or dense low k dielectric layer on a substrate;
[0019] b) forming single or dual damascene etched openings in the low k dielectric;

[0020] c) placing the substrate in a process chamber on a cold chuck at a temperature about -200.degree. C. to about 25.degree. C.;

[0021] d) adding to the process chamber a condensable cleaning agent (CCA) to condense a layer of CCA within the etched openings on the substrate; and

[0022] e) performing an activation step while the wafer remains cold at a temperature of about -200.degree. C. to about 25.degree. C.

[0023] The present invention further provides a method of making a BEOL interconnect structure including a porous or dense low k dielectric having low via contact resistance. The method includes the steps of:

[0024] a) forming a porous or dense low k dielectric layer on a substrate;

[0025] b) forming single or dual damascene etched openings in the low k dielectric;

[0026] c) placing the substrate in a first process chamber on a cold chuck at a temperature about -200.degree. C. to about 25.degree. C.;

[0027] d) adding to the first process chamber a condensable cleaning agent (CCA) to condense a layer of CCA within the etched openings on the substrate;

[0028] e) moving the substrate to a second process chamber on a cluster tool; and

[0029] f) performing an activation step in the second process chamber.

[0030] The present invention still further provides a BEOL interconnect structure including a porous or dense low k dielectric having low via contact resistance prepared by the above methods of the present invention.

[0031] The via contacts prepared by the methods of the present invention are very stable during thermal cycles and during operation of the semiconductor device. Further, the via contacts prepared by the methods described herein have a lower resistance than the vias described in the prior art. In addition, in the present invention, the vias are surrounded by a liner (for example, see element 6 in FIG. 1) and the adhesion of the liner is stronger than it is in the vias described in the prior art. As a result, the interconnect structures of the present invention are more reliable and more stable than the

interconnect structures of the prior art, because stronger liner adhesion leads to more reliable and stable interconnect structures.

[0043] Referring to FIG. 1, an example of dual damascene level is described in which a substrate 10 and an etch stop/barrier layer 2 are shown. On the etch stop/barrier is deposited the ILD 3 and an optional hardmask 4 is atop the ILD. It should be noted that the hardmask can be composed of a single or multiple layers to form a composite hardmask film. A Cu conductor 5 is formed within the ILD, separated from the ILD by the liner/Cu diffusion barrier 6.

[0044] A second etch stop/barrier layer 7 forms the "cap" on the Cu conductor. Each of the metallic lines and vias 5 can optionally include a liner material 6, which lines the metallic lines and vias.

[0045] Suitable materials that can be used as liners include, but are not limited to, TiN, TaN, Ta, WN, W, TaSiN, TiSiN, WCN, Ru and the like and mixtures thereof. **The liner can be a single layer or it can include multiple layers.**

[0059] Suitable dielectrics for layer 30 are porous or dense inorganic materials including, but not limited to, silicon-containing materials such as compositions formed from one or more of Si, C, O, F and H, e.g., FSG, C doped oxide, F doped oxide, alloys of Si, C, O and H and the like. Specific examples of PE CVD materials of the composition Si, C, O, and H include, but are not limited to, Black Diamond from Applied Materials, Coral from Novellus Systems and Aurora from ASM., all have k approximately 3.0, and include the range 2.8 to 3.2. Also, SiCOH dielectrics containing porosity and having k from 2.7 down to 1.8 may be preferably used within this invention, including BDII and BDIII from Applied Materials, Aurora ULK and ELK from ASM, and other porous SiCOH films. A variety of spin applied films having the composition Si, C, O, H, such as, methylsilsesquioxanes, siloxanes and 5109, 5117, 5525, 5530 from Japan Synthetic Rubber (JSR), and Dendriglass may also be used. The materials known as Orion and other materials from Trikon may also be used.

[0060] Techniques and parameters for forming first dielectric layer 30 on substrate 110 (e.g., PE CVD or spin coating) are within the purview of one skilled in the art. As is known in

the art, PECVD from a cyclic precursor and a second hydrocarbon precursor is one preferred method to make SiCOH dielectrics with k between 2 and 3, as disclosed in U.S. Pat. Nos. 6,312,793; 6,441,491; and 6,479,110 B2, the contents of which are incorporated herein by reference.

Therefore, it would have been obvious to one of ordinary skill in the art to use the liner barrier layer and the thin dielectric layer as "merely a matter of obvious engineering choice" as set forth in the above case law.

Initially, and with respect to claim 8, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Grunow et al. (U.S. Application Publication # 2005/0082089 A1).
8. The interconnect structure of claim 1, Grunow et al. show wherein the TDL is deposited by a method selected from the group consisting of: high density plasma (HDP), downstream HDP, electron cyclotron resonance (ECR), plasma enhanced chemical vapor deposition (PE CVD), assisted PE CVD, and plasma enhanced atomic layer deposition (PE ALD).

As to the grounds of rejection under section 103 in claim 8, see MPEP § 2113.

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Beyer et al. (U.S. Patent Application Publication # 2005/0074961 A1).
8. The interconnect structure of claim 1, Beyer et al. show wherein the TDL is deposited by a method selected from the group consisting of: high density plasma (HDP), downstream HDP, electron cyclotron resonance (ECR), plasma enhanced

chemical vapor deposition (PE CVD), assisted PE CVD, and plasma enhanced atomic layer deposition (PE ALD).

As to the grounds of rejection under section 103 in claim 8, see MPEP § 2113.

Claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Any such indication as to the allowability of these claims is reserved until which time a suitable response is filed.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/700-703,758,751,774,773, 174/266,257 29/831	1/21/06
Other Documentation: foreign patents and literature in 257/700-703,758,751,774,773, 174/266,257 29/831	1/21/06
Electronic data base(s): U.S. Patents EAST	1/21/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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